PATENT
Attorney Docket No. 401558/SAKAI

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

TAKAO HASEGAWA

Application No. Unassigned

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Art Unit: Unassigned

Examiner: Unassigned

For: METHOD OF WIRING SEMICONDUCTOR INTEGRATED CIRCUIT, SEMICONDUCTOR INTEGRATED CIRCUIT, AND COMPUTER PRODUCT

PENDING CLAIMS AFTER ENTRY OF PRELIMINARY AMENDMENT

1. A method of wiring a semiconductor integrated circuit having a first layer and a second layer, the method comprising:

disposing a first wiring on a first layer of a semiconductor integrated circuit and disposing a second wiring on a second layer of said semiconductor integrated circuit, wherein said first and second wirings are arranged subject to a condition that a predetermined number of through-holes are to extend between said first and second wirings, connecting said first and second layers to each other;

searching for a setting area in one of said first and second layers, and a corresponding area in the other of said first and second layers as a projection of the setting area, that enable setting of an additional through-hole between said first and second wiring; and

setting the additional through-hole between the setting area and the corresponding area.

2. The method of wiring a semiconductor integrated circuit according to claim 1, wherein, in setting the additional through-hole, giving the additional through-hole the same shape as the predetermined number of through-holes.

3. The method of wiring a semiconductor integrated circuit according to claim 1, wherein, in setting the additional through-hole, choosing shape of the additional through-hole based on shape of the setting area.

4. A method of wiring a semiconductor integrated circuit having a first layer and a second layer, the method comprising:

disposing a first wiring on a first layer of a semiconductor integrated circuit and disposing a second wiring on a second layer of said semiconductor integrated circuit, wherein said first and second wirings are arranged subject to a condition that a predetermined number of through-holes are to extend between said first and second wirings, connecting said first and second layers to each other;

searching for a setting area in said first layer, and a corresponding area in said second layer as a projection area of the setting area, that enable setting of an additional through-hole between said first and second wiring;

disposing an additional wiring for setting the additional through-hole in either the setting area or the corresponding area; and

setting the additional through-hole to extend between the setting area and the corresponding area.

5. The method of wiring a semiconductor integrated circuit according to claim 4, wherein,

in searching for a setting area, searching under a condition that the setting area is a part of the area in which said first wiring has been disposed, and that the corresponding area is an area that is close to said second wiring and an area in which no wiring or circuit element exists, and

in arranging the additional wiring, extending said second wiring to the corresponding area.

6. The method of wiring a semiconductor integrated circuit according to claim 4, wherein,

in searching for a setting area, searching under a condition that the setting area is an area that is close to said first wiring on said first layer and in which no wiring or circuit element exists, and the corresponding area is an area that is close to said second wiring on said second layer and in which no wiring or circuit element exists, and

in disposing the additional wiring, extending said first wiring on said first layer to the setting area, and extending said second wiring on said second layer to the corresponding area.

7. The method of wiring a semiconductor integrated circuit according to claim 4, wherein, in setting the additional through-hole, making the shape of the additional through-hole the same as the shape of through-hole.

8. The method of wiring a semiconductor integrated circuit according to claim 4, wherein, in setting the through-hole, choosing a shape of the additional through-hole based on shape of the setting area.

9. A semiconductor integrated circuit comprising:

a multi-layer structure including a first layer and a second layer;

a setting area disposed on said first layer;

a corresponding layer disposed on said second layer as a projection of said setting area; and

a through-hole which connects said setting area and said corresponding area, said through-hole having a shape corresponding to shapes of said setting area and said corresponding area.

10. A computer program containing instructions which, when executed on a computer causes the computer to design wiring of a semiconductor integrated circuit, having a first layer and a second layer, the method comprising:

disposing a first wiring on a first layer of a semiconductor integrated circuit and disposing a second wiring on a second layer of said semiconductor integrated circuit, wherein said first and second wirings are arranged subject to a condition that a predetermined number of through-holes are to extend between said first and second wirings, connecting said first and second layers to each other;

searching for a setting area in one of said first and second layers, and a corresponding area in the other of said first and second layers as a projection of the setting area, that enable setting of an additional through-hole between said first and second wiring; and

setting the additional through-hole between the setting area and the corresponding area.

11. A computer program containing instructions which when executed on a computer, causes the computer to design wiring of a semiconductor integrated circuit, having a first layer and a second layer, the method comprising:

disposing a first wiring on a first layer of a semiconductor integrated circuit and disposing a second wiring on a second layer of said semiconductor integrated circuit, wherein said first and second wirings are arranged subject to a condition that a predetermined number of through-holes are to extend between said first and second wirings, connecting said first and second layers to each other;

searching for a setting area in said first layer, and a corresponding area in said second layer as a projection area of the setting area, that enable setting of an additional through-hole between said first and second wiring;

disposing an additional wiring for setting the additional through-hole in either the setting area or the corresponding area; and

setting the additional through-hole to extend between the setting area and the corresponding area.